REMARKS

Reconsideration of this application as amended is respectfully requested.

In the Office Action, claims 1-71 are pending. Claims 1-71 stand rejected. In this response, claims 1, 3, 5, 12-15, 24, 29-30, 33-34, 40, 45-46, 49-50, 56, 61-62 and 65-66 have been amended. No new claims have been added. No claims have been canceled. Thus, claims 1-71, as amended, remain pending. Support for the amendments can be found throughout the specifications as filed. No new matter has been added. Applicants reserve all rights with respect to the applicability of the Doctrine of Equivalents.

Amendments

Amendments to the Claims

Objections

Claims **2, 3, 5, 12, 13, 14, 15, 30, 33, 34, 46, 49, 50, 61, 62, 65 and 66**

Claims 2, 3, 5, 12, 13, 14, 15, 30, 33, 34, 46, 49, 50, 61, 62, 65 and 66 are objected to because of the informalities of the claim language "capable." Applicants have corrected the informalities in claims 1, 3, 5, 12-15, 30, 33-34, 45-46, 49-50, 61-62 and 65-66, as amended, by deleting the phrase "being capable of". Applicants assert that claim 2 positively recite the claimed scope without informalities in the claim language. Accordingly, withdrawal of the objections is respectfully requested.

Rejections

Rejections under 35 U.S.C. § 102(b)

Claims **1-2, 9-13, 19-22, 24-25, 27-29, 33, 37-41, 43-45, 49, 54-56, 59-61, 65, 70-71**

Claims 1-2, 9-13, 19-22, 24-25, 27-29, 33, 37-41, 43-45, 49, 54-56, 59-61, 65, 70-71 stand rejected under 35 U.S.C. §102(b) as being anticipated by John Liang Wing So, US Patent No. 5,909,559 (hereinafter "So"). However, applicants respectfully submit that

applicants' claims 1-2, 9-13, 19-22, 24-25, 27-29, 33, 37-41, 43-45, 49, 54-56, 59-61, 65, 70-71, as amended, are not anticipated by the cited reference.

Specifically, for example, independent claim 1, as amended, includes the limitations:

> "a chip interconnect;
> a host interface coupled to the chip interconnect for interfacing the IC with the at least one host processor external to the IC;
> a memory interface coupled to the chip interconnect for accessing a memory external to the IC, the memory interface including a non-coherent interface for interfacing the IC with the host memory external to the IC, the memory interface including a coherent interface for interfacing a cache memory external to the IC via the at least one host processor;
> a memory controller coupled to the chip interconnect for controlling the host memory comprising DRAM memory via the memory interface, the memory controller to determine whether to access the memory through the coherent interface or the non-coherent interface;
> a scalar processing unit coupled to the chip interconnect, the scalar processing unit executing instructions to perform scalar data processing;
> a vector processing unit coupled to the chip interconnect, the vector processing unit executing instructions to perform vector data processing; and
> an input and output (I/O) interface coupled to the chip interconnect for interfacing the IC with an I/O controller of the data processing system, the I/O controller being external to the IC for controlling I/O devices of the data processing system, wherein the chip interconnect, the memory controller, the scalar processing unit, the vector processing unit, the I/O interface, the host interface, and the memory interface are implemented within the IC which is a single chipset interfacing the at least one host processor and the host memory with other components of the data processing system, including the I/O controller and the I/O devices"
> (emphasis added)

Applicant's amended claim 1 includes the limitations of determining to access a memory external to an IC through a coherent interface in a memory interface interfacing a cache memory external to the IC via a host processor external to the IC. It is respectfully submitted that So lacks the above noted limitations.

Rather, So discloses an integrated circuit providing on a single chip for use with an off-chip processor with first terminals for the processor related signals, second terminal for external bus-related signals, and third terminals for memory-related signals and a memory controller connected to the third terminals (So, Abstract). In So, a host CPU (i.e. off-chip processor) with multimedia extension MMX is coupled to an embedded L2 cache and

additionally to a main memory via a north bridge chip (So, col. 130, lines 18-21, Fig. 1). So also describes a north bridge embodiment (i.e. the chip) having five ports for CPU (Central Processing Unit), AGP (Advanced Graphics Port), PCI (Peripheral Component Interconnect), VSP (wrapper-and-DSP-core) and memory I/F (Interface) (So, col. 127, lines 31-35, Figs. 22, 126, 127). VSP port, PCI port, CPU port and AGP port, according to So, are multiplexed into an memory arbiter with a crossbar switch or a data bus multiplexer (So, col. 127, lines 41-44). The memory arbiter arbitrates among the CPU, AGP, PCI, and VSP ports for memory access (So, col. 127, lines 38-39). However, So is completely silent about determining to access a memory external to an IC through a coherent interface in a memory interface interfacing a cache memory external to the IC via a host processor external to the IC.

In order to anticipate a claim, each and every limitation of the claim must be taught by the cited reference. It is respectfully submitted that So fails to disclose the limitations set forth above. Therefore, it is respectfully submitted that independent claim 1, as amended, is not anticipated by So.

Independent claims 24, 40 and 56, as amended, include similar limitations as noted above. Therefore, for at least the similar reasons as discussed above, it is respectfully submitted that claims 24, 40 and 56, as amended, are not anticipated by So.

Given that claims 2, 9-13, 19-22, 25, 27-29, 33, 37-39, 41, 43-45, 49, 54-55, 59-61, 65 and 70-71, as amended, depend from and include all limitations of one of independent claims 1, 24, 40 and 56, as amended, applicants respectfully submit that claims 2, 9-13, 19-22, 25, 27-29, 33, 37-39, 41, 43-45, 49, 54-55, 59-61, 65 and 70-71, as amended, are not anticipated by So.

Rejections Under 35 U.S.C. 103(a)

Claims **3, 4, 26, 42 and 58**

Claims 3, 4, 26, 42 and 58 stand rejected under 35 U.S.C. §103(a) as being unpatentable over So in view of Steven G. Morton, US Patent No 5,822,606 (hereinafter "Morton"). However, applicants respectfully submit that applicants' claims 3, 4, 26, 42 and 58, as amended, are patentable over the cited references.

It is respectfully submitted that neither So, for reasons similar to those discussed above, nor Morton, individually or in combination, disclose or suggest the above noted limitations of independent claims 1, 24, 40 and 56, as amended.

Morton teaches a parallel DSP (Digital Signal Processing) chip including a memory interface, parallel DMA (Direct Memory Access) data ports and a parallel DMA control port (Morton, col. 9, lines 40-59, Fig. 1). Morton also discloses the memory interface connects the parallel DSP chip to an external random access memory (Morton, col. 9, lines 60-62). According to Morton, data are sent from a parallel DMA port (i.e. a parallel DMA control port or a parallel DMA data port) to an I/O data bus and received by a parallel DMA port from an I/O data bus (Morton, col. 11, lines 42-58). Additionally, Morton states that a DMA controller inside a parallel DMA port selects word for reading or writing so that an external I/O device needs only to supply or absorb a stream of data without providing addresses (Morton, col. 11, lines 36-39). However, nowhere does Morton disclose or suggest determining to access a memory external to an IC through a coherent interface in a memory interface interfacing a cache memory external to the IC via a host processor external to the IC.

Further, So is related to integrated circuits and computer system embodiments for desktop and mobile computers, television sets, set-top boxes and appliances improved with asymmetrical multiprocessors (So, col. 129, lines 22-26). Mortan, however, relates to semiconductor device designed for the processing of data in a parallel fashion (Morton, col. 1, lines 64-66). Asymmetrical processing and parallel processing belong to two different arts. There is neither suggestion nor motivation to combine So and Morton.

As such, not only do So and Morton not disclose, individually or even in combination, the above noted limitations, but the references, considered as a whole, do not suggest the desirability and thus the obviousness of making the combination. It would be impermissible hindsight to combine So and Morton based on applicants' own disclosure. Even if they are combines, such a combination still lacks the limitations set forth above.

In order to render a claim obvious, each and every limitation of the claim must be taught by the cited references. Therefore, in view of the foregoing remarks, it is respectfully submitted that independents 1, 24, 40 and 56, as amended, are patentable over So and Morton.

Given that claims 3, 4, 26, 42 and 58, as amended, depend from one of independent claims 1, 24, 40 and 56, as amended, for at least the reasons similar to those discussed above, it is respectfully submitted that claims 3, 4, 26, 42 and 58 are patentable over the cited references.

Claims **14-18, 34-36, 50-52, and 66-68**

Claims 14-18, 34-36, 50-52 and 66-68 stand rejected under 35 U.S.C. §103(a) as being unpatentable over So in view of Eric M. Dowling, US Patent No 6,597,745 (hereinafter "Dowling"). Applicants hereby reserve the right to swear behind Dowling at a later date. However, applicants respectfully submit that applicants' claims 14-18, 34-36, 50-52 and 66-68, as amended, are patentable over the cited references.

It is respectfully submitted that neither So, for reasons similar to those discussed above, nor Dowling, individually or in combination, disclose or suggest the above noted limitations of independent claims 1, 24, 40 and 56, as amended.

Dowling teaches systems and methods to precode a transform-domain vector communication signal such as block of Hermitian-symmetric DMT (Discrete Multitone Modulation) signal points with a reduction in computational complexity (Dowling, col. 2, lines 59-62). Dowling also describes a Hermitian-symmetric frequency domain vector of DMT signal points, belonging to a set of N-dimensional vectors whose elements are defined over the complex integers, is applied to an input of a combining unit (Dowling, col. 3, lines 60-63, col. 4, lines 2-4, Fig. 1). Additionally, Dowling discloses a system including exchange-permutation operations involving an upper-triangular Toeplitz matrix (Dowling col. 13, lines 55-63, Fig. 4). However, nowhere does Dowling disclose or suggest determining to access a memory external to an IC through a coherent interface in a memory interface interfacing a cache memory external to the IC via a host processor external to the IC.

Further, Dowling is related to data transmission for multicarrier systems (Dowling, col. 1, liens 7-10). So, however, relates to integrated circuits and computing system embodiments for desktop and mobile computers, television sets, set-top boxes and appliances improved with asymmetrical multiprocessors (So, col. 129, lines 22-26). Thus, Dowling and

So belong to completely different arts. There is neither suggestion nor motivation to combine So and Dowling.

As such, not only do So and Dowling not disclose, individually or even in combination, the above noted limitations, but the references, considered as a whole, do not suggest the desirability and thus the obviousness of making the combination. It would be impermissible hindsight to combine So and Dowling based on applicant's own disclosure. Even if they are combines, such a combination still lacks the limitations set forth above.

In order to render a claim obvious, each and every limitation of the claim must be taught by the cited references. Therefore, in view of the foregoing remarks, it is respectfully submitted that independents 1, 24, 40 and 56, as amended, are patentable over So and Dowling.

Given that claims 14-18, 34-36, 50-52 and 66-68, as amended, depend from one of independent claims 1, 24, 40 and 56, as amended, for at least the reasons similar to those discussed above, it is respectfully submitted that claims 14-18, 34-36, 50-52 and 66-68 are patentable over the cited references.

CONCLUSION

In view of the foregoing, applicant respectfully submits the applicable rejections and objections have been overcome. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call the undersigned attorney at (408) 720-8300.

Please charge Deposit Account No. 02-2666 for any shortage of fees in connection with this response.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

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Vincent WenJeng Lue
Reg. No. 56,564
Vincent_Lue@bstz.com

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025-1026
(408) 720-8300